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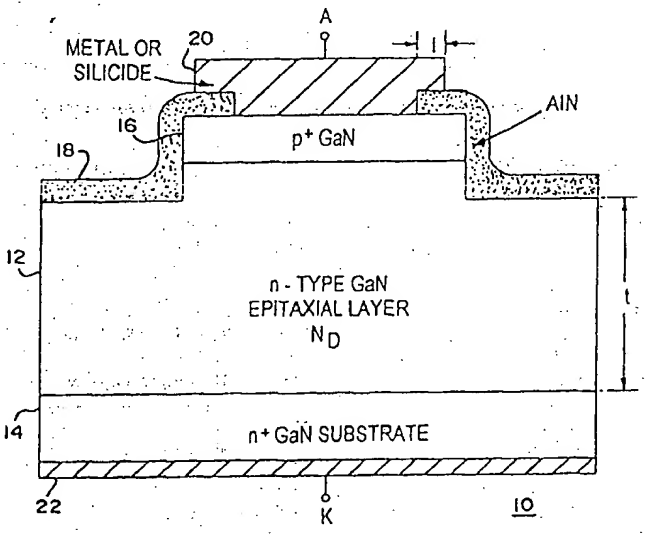


(57) Abstract

A semiconductor charge-control device (10) is provided. The device includes a first layer (12) of a Periodic Table Group III nitride of a first conductivity type and a first doping level which forms a drift region of the semiconductor charge-control device and a second layer (16) of the Periodic Table Group III nitride of a second conductivity type and a second doping level at least one order of magnitude above the first doping level, said second layer being disposed on a first side of the first layer. The device also includes a third layer (14) of the Periodic Table Group III nitride of the first conductivity tyc and a doping level of at least twice the doping level of the first layer, said third layer being disposed on the second side of the first layer.

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# SOLID STATE POWER-CONTROL DEVICE USING GROUP III NITRIDES

## Field of the Invention

The field of the invention relates to semiconductors and, more particularly, to power-control transistors.

## Background of the Invention

Diodes, silicon controlled rectifiers (SCRs) and power transistors, such as gate turn-off transistors (GTOs) and insulated gate bipolar transistors (IGBTs), are generally known in the field of power control. IGBTs are generally known to be high voltage (e.g., 500 volts, or more), high power devices (e.g., 1 kW, or more) that have a great deal of usefulness in a number of fields (e.g., motor controls, rectifiers, etc.).

IGBTs are usually constructed in the form of a 4-layer device similar to a SCR. As is the case with SCRs, once early IGBTs were triggered into a conductive state, the presence of regenerative currents within the IGBT would tend to maintain the IGBT in a conductive state, resulting in a loss of gate control. This condition is generally referred to as "latch-up". In an effort to improve the usefulness of IGBTs, recent advances have included the creation of punch-through IGBTs having a buffer layer in a drift region, adjacent the collector, which interferes with regenerative currents, thereby reducing the likelihood of latch-up.

Where latch-up can be controlled, an IGBT can be created which has the ability of turning off under load. The ability to turn off under load makes an IGBT much more useful as a power control unit in such devices as inverters or power controllers.

While latch-up can generally be controlled, one of the remaining difficulties with the use of IGBTs is the inefficiencies of IGBTs associated with their slow turn-off times and internal resistance. IGBTs and diodes rely on a relatively thick drift region of doped silicon to resist electrical breakdown. With a generally accepted electrical breakdown voltage rating of 10 volt/$\mu$m within the drift region of silicon, a 1000 volt device generally requires a drift region of the order of 100 $\mu$m. The relatively thick drift region for silicon and high bulk resistance of silicon limits the current handling capacity of devices made of silicon. The relatively thick drift region also provides a significant charge reservoir during conduction and a source of difficulty in charge removal during turn-off.

The presence of charge carriers (e.g., electrons and holes) in the drift region is necessary for device conduction. When charge remains in the drift region after removal of control voltage from an IGBT gate connection, current continues to flow through the drift region and, consequently, through the IGBT. As charge depletion gradually occurs during turn-off, a voltage builds up across the IGBT, eventually resulting in turn-off of the device. During turn-off, the power dissipated within the IGBT is determined by the product of current times voltage, according to well-known principles.

While IGBTs have proven useful in inverters and elsewhere, their use is still limited to applications involving switching rates of less than 100 kHz. At frequencies above 100 kHz, the power dissipated during switching can result in overheating and, ultimately, device failure.

Efforts to improve device turn-off times have included the use of carrier lifetime control within the drift region.

Carrier lifetime control, as that term is used in the art, refers to the creation of sites within the structure of the IGBT or diode that facilitates the re-combination of electrons and holes. Lifetime control may include the dispersion of an appropriate material (e.g., gold particles) through the silicon lattice of the substrate or irradiation. Irradiation of the substrate purposefully damages the crystal structure in such a way as to facilitate charge re-combination.

While lifetime control is effective to some degree in increasing the speed of turn-off, lifetime control also has the effect of increasing device resistance. Increasing device resistance also causes heat generation and heat build-up within the IGBT or diode during normal current flow. Increasing the lifetime control through metallic dispersions or irradiation, while allowing for an increase in maximum switching speeds, results in a trade-off which can cause an overall decrease in device efficiency.

Accordingly, it is an object of the invention to provide a semiconductor structure with improved breakdown strength, reduced electrical and heat flow resistance and faster turn-off times.

It is a further object of the invention to provide a mechanism for rapid charge depletion within the drift region after turn-off of the device that does not result in an overall increase in device resistance.

It is a further object of the invention to provide a structure for IGBTs that is applicable for punch through IGBTs and non-punch through IGBTs.

## Summary

In one embodiment of the invention, an improved semiconductor charge-control device is provided. The device

includes a first layer of a Periodic Table Group III nitride (such as GaN) of a first conductivity type and a first doping level which forms a drift region of the semiconductor charge-control device and a second layer of a second conductivity type and a second doping level, said second layer being disposed on a first side of the first layer. The device also includes a third layer of the Periodic Table Group III nitride of the first conductivity type and a doping level of at least twice the doping level of the first layer, said third layer being disposed on the second side of the first layer.

## Brief Description of the Drawings

FIG. 1 is a cut-away view of a GaN diode in accordance with an embodiment of the invention;

FIG. 2 is a cut-away view of a hybrid GaN/SiC diode using a SiC substrate in accordance with an alternate embodiment of the invention;

FIG. 3 is a cut-away view of the diode of FIG. 2 with an added buffer layer;

FIG. 4 depicts electrical characteristics of the diode of FIG. 3 for varying layer thicknesses;

FIG. 5 depicts electrical characteristics of the diode of FIG. 3 for varying doping levels;

FIG. 6 depicts application ranges for the diodes of FIGs. 1 and 3 with a minimum Group III-nitride doping level of $1x10^{16}$ $cm^{-3}$;

FIG. 7 provides comparative I-V data for a GaN 4.5 kV diode of FIGs. 1 and 2 and similar SiC and Si diodes;

FIG. 8 provides comparative I-V data for a GaN 10 kV diode of FIGs. 1 and 2 and, a similar SiC diode, and a GaN/SiC diode of the type shown in Fig. 3;

FIG. 9 depicts a doping level distribution for a 4.5 kV GaN diode of FIG. 1 and for SiC;

FIG. 10 depicts a doping level distribution for a 10 kV GaN diode such as those shown in of FIGs. 1 and 2, a GaN/SiC diode such as that shown in FIG. 3, and for a SiC diode;

FIG. 11 depicts reverse recovery characteristics for a 4.5 kV diode of FIG. 1;

FIG. 12 depicts reverse recovery characteristics for a 10 kV diodes of FIGs. 1, 2 and 3;

FIG. 13 depicts a MISFET in accordance with an alternate embodiment of the invention;

FIG. 14 depicts a hybrid MISFET in accordance with an alternate embodiment of the invention;

FIG. 15 depicts the hybrid MISFET of FIG. 14 with an added buffer layer;

FIG. 16 depicts an IGBT in accordance with an alternate embodiment of the invention;

FIG. 17 depicts a hybrid IGBT in accordance with an alternate embodiment of the invention; and

FIG. 18 depicts the hybrid IGBT of FIG. 17 with an added buffer layer.

## Detailed Description of the Invention

FIG. 1 depicts a GaN diode under an embodiment of the invention. Under the embodiment, the operative parts of the power control device (e.g., the diode 10 of FIG. 1) are constructed of a material much better suited to adverse environments.

Under the embodiment, device efficiency and reliability is significantly increased through the use of a Periodic Table Group III nitride (e.g., GaN) at the charge-control junction. The use of GaN has been found to provide superior performance in the operation of semiconductor devices.

For example, it has been found that the wide bandgap between valence and conduction bands of GaN allows a GaN device to be successfully used up to 600°C. Prior art silicon or GaAs devices cannot be used above 150°C due to the uncontrolled generation of intrinsic carriers.

Further silicon and GaAs cannot tolerate chemically hostile environments. In contrast, GaN is mechanically and chemically resistant to most environmental conditions.

Table I provides a comparison of GaN with silicon and also with silicon-carbide (SiC). As shown GaN has a breakdown dielectric field strength $E_M$ which is more than an order of magnitude higher than Si.

Table I

| Material | $N_D(cm^{-3})$ | W(μm) | τ(ns) | $E_M(V/cm)$ | $\sigma_A(Wcm)^{-1}$ |
|---|---|---|---|---|---|
| Si | $2.9x10^{13}$ | 400 | 10,000 | $1.8x10^5$ | 0.174 |
| SiC | $2.5x10^{15}$ | 40 | 500 | $1.8x10^6$ | 33 |
| GaN | $1.0x10^{16}$ | 20 | 10 | $3.7x10^6$ | 800 |

Since the breakdown voltage is much higher for GaN than silicon (or SiC), it is possible to make the drift region 12 of FIG. 1 much thinner than a comparable silicon device. Further, since the conductance $\sigma_A$ is also much larger for GaN than silicon, an allowable current density can be much higher for GaN than silicon (or SiC).

GaN has a relatively short carrier lifetime. The low lifetime of GaN makes it a somewhat inefficient semiconductor for the construction of bipolar power switching devices since it is somewhat difficult to obtain high-level injection or high conductivity modulation. However, high carrier mobility and high breakdown field strength (compared to Si or SiC) allows GaN to be a much

better switching device than Si or SiC. Further, the method described below for creating an electrically transparent GaN/SiC heterojunction allows the benefits of both materials to be available in the same hybrid device.

Turning now to FIG. 1, the GaN diode 10 of FIG. 1 may be fabricated under any of a number of techniques including both diffusion and deposition steps (e.g., metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), chemical vapor deposition (CVD), HVPE, etc.). Under one embodiment, an n+ substrate 14 of GaN may be deposed on sapphire ($Al_2O_3$) using an epitaxial process (e.g., HVPE). N-type dopants may be added as a dopant (e.g., to n+ doping level of 1e19/cm-3) during the deposition process. The sapphire may be etched away in later processing steps to leave the structure 14 shown in FIG. 1.

Under the embodiment the n+ substrate 14 of FIG. 1 may also be deposited on sapphire over an intermediate layer of ZnO using HVPE. Even though ZnO is somewhat unstable at high temperatures, the rapid coverage by GaN prevents decomposition of the ZnO. After growing a GaN layer about 300 μm thick, the sapphire substrate may be removed either chemically or mechanically.

The sapphire substrate is removed because of a lattice mismatch in the structure of the GaN and sapphire. Growing the GaN to a greater thickness may result in the accumulation of stress, which may result in cracking during the epitaxial process.

Following creation of the substrate 14, a second n-type epitaxial layer 12 is created on top of the first layer 14. The second layer forms a drift region of GaN of a second doping level (e.g., 1e16/$cm^{-3}$).

To achieve a set of desirable characteristics for the GaN drift region 12, it has been found that the residual

doping level of the GaN must be carefully controlled. Residual n-type doping in GaN has been recognized to arise from both native defects (nitrogen vacancies and interstitial gallium) and impurities (O and Si) introduced by the carrier and the active gases. It has been found that the residual doping level can be reduced by carefully regulating the control of the carrier and active gases using the process recipe. The density of native defects can also be reduced by careful attention to the stoichiometry of the gas phase (ratio of partial pressure of NH3 to partial pressure of GaCl, V/III). Within growth conditions necessary for maintaining good surface morphology, the ratio V/III can be used to achieve the lowest residual native defect density.

To further reduce the free carrier concentration, an additional Mg source is added to compensate for a portion of the residual n-type doping. This is at the expense of carrier mobility, but since Mg is one of the shallowest p-type impurity, this decrease is limited. Furthermore, low Mg doping does not introduce deep states. Both carrier mobility and lifetime are strongly dependent upon the crystalline quality (i.e., defect density) of the semiconductor from which the device is fabricated. In wide bandgap materials, the defect density may determine whether carrier transport is due to an insulator-like hopping mechanism or to a more conventional continuous band-like transport mechanism associated with metals and semiconductors.

Following creation of the drift region, the device 10 may be masked and a p+ anode 16 created by diffusion. The p+ anode 16 may be created by diffusing a p-type material into a selected area to an appropriate doping level (e.g.,

1e19 $cm^{-3}$). This p+ region can also be formed by deposition techniques such as MOCVD and MBE.

Following deposition of the drift region 12 and p+ anode 16, the surface of the device 10 may be masked again and an insulating layer 18 of aluminum-nitrite (AlN) or a dielectric deposited around the p+ diffusion location 16. A metal or silicide connection 20 may then be deposited over the p+ material 16 to form the anode 20 of the diode 10. As a final step a metal or silicide cathode 22 may be deposed over the lower surface of the device 10.

FIG. 2 shows a diode 20 under another embodiment of the invention. Under the embodiment, a substrate 34 of silicon-carbide is provided to further enhance the performance of the diode 30. The SiC substrate 34 may be created using known techniques. The GaN drift region 32 may then be epitaxially deposited on the substrate 34 either directly or through the use of interfacial layers as described above. Other interfacial layers such as SiTe may also be worked to obtain an improved lattice match.

Further, the SiC substrate 32 may be thermally etched and additional SiC layers may be epitaxially deposited to improve the surface roughness prior to heteroepitaxy of GaN. An interfacial layer of SiTe may then be added to improve lattice matching.

In addition to lattice matching, control of the interface is also important in terms of reducing the trap density at the interface. Several unique Al and Te precursors may be useful in reducing the trap at the SiC/GaN interface. SiC/$SiTe_2$ is believed to be the most useful in the epitaxial growth of GaN. A GaN epilayer covalently bonded to the uppermost Te atomic layer of the substrate 34 is then able to grow with its natural lattice constant. This is believed to be due to the graphite-like structure

between any adjacent pair of Te atomic layers resulting in relatively weak Van der Waals bonding between them. Hence, the lattice mismatch between GaN and Si is full compensated for by the sliding of one Te layer relative to another. In situ photoemission measurements have been found to be useful in studying the band offset at the interface.

The GaN layer provides high electrical conductivity, high avalanche field strength, and superior optical characteristics. The n-type SiC layer can be used either as a buffer layer (thin layer) 26, as in FIG. 3, to control the injection efficiency and carrier recombination or to also support the electric field and provide low electrical resistance in the high-level injection regime when sufficiently thick.

The SiC material further improves the overall thermal performance of this structure. The SiC has a thermal conductivity 3-4 times that of GaN and when combined with GaN functions to lower an overall operating temperature of the GaN.

Where SiC is used as a buffer layer 26 (FIG. 3) to control carrier recombination, the buffer layer 26 may also be subject to certain additional steps to facilitate recombination. Lifetime control may include a dispersion of an appropriate material (e.g., gold particles) within the buffer region 26. Irradiation of the buffer layer 26 may be used to facilitate recombination by purposely damaging the structure of the region 26.

FIG. 4 shows the relationship of specific on-state resistance to diode breakdown voltage $V_{BD}$. Also plotted is the fractional voltage that may be supported by a thin GaN layer. FIG. 5 illustrates how the doping of the SiC layer may be changed to support the required voltage and also the GaN layer thickness.

FIG. 6 shows the ratio of on-state resistance $R_{ON}$ of a hybrid GaN/SiC diode 30 to that of the SiC diode with identical voltage ratings. Also illustrated is a range of $V_{BD}$ that can be achieved with a GaN/SiC device 30 with at least 50% lower resistance $R_{ON}$ compared to a diode of SiC alone, based on a GaN doping density of $1x10^{16}$ $cm^{-3}$.

FIG. 7 shows forward voltage drop of the GaN diode 10 of FIG. 1 compared to a Si diode and a SiC diode. As shown, the 4.5 kV GaN diode 10 provides a dramatic forward voltage drop reduction over Si and SiC. FIG. 8 shows forward voltage drop for a 10 kV diode of FIGs. 1-3. FIGs. 9 and 10 show carrier concentrations for the 4.5 and 10 kV diodes, respectively.

Table I indicates that a net carrier lifetime $\tau$ of GaN is three orders of magnitude lower than silicon. The effect of the faster carrier lifetime can be seen in the turn-off time of the 4.5 kV diodes in FIG. 11. The turn-off times of the 10 kV diodes can be seen in FIG. 12.

Table II shows electrical loss for a 4.5 kV diode. As shown SiC has a lower turn-on loss than GaN, but a higher total loss. This is because although SiC has a lower reverse current peak than Si, it has a much longer current tail. This shows up as a large turn-off loss.

TABLE II

| Material | Turn-On Loss | Cond. Loss | Turn-Off Loss | Total Loss |
|---|---|---|---|---|
| Si | 374 µJ | 1000 µJ | 1296 µJ | 2669 µJ |
| SiC | 9 µJ | 299 µJ | 284 µJ | 592 µJ |
| GaN | 19 µJ | 491 µJ | 1 µJ | 511 µJ |
| Hybrid | N/A | N/A | N/A | N/A |

Table III is a compilation of losses for a 10 kV diode. As should be noted, even though GaN has a lower overall loss, it still has a higher conduction loss than the hybrid of GaN and SiC.

TABLE III

| Material | Turn-On Loss | Cond. Loss | Turn-Off Loss | Total Loss |
|---|---|---|---|---|
| Si | N/A | N/A | N/A | N/A |
| SiC | 9 μJ | 320 μJ | 2936 μJ | 3265 μJ |
| GaN | 4 μJ | 480 μJ | 33 μJ | 517 μJ |
| Hybrid | 32 μJ | 436 μJ | 133 μJ | 601 μJ |

GaN has higher carrier mobility and breakdown field strength than SiC. However, it has poor thermal conductivity. Moreover, the lowest achievable doping presently available for GaN is in the range of 1e16 $cm^{-3}$, which corresponds to a breakdown voltage of 4.5 kV. The hybrid device 30 exploits the superior properties of both GaN and SiC devices. In order to achieve higher breakdown voltage levels, SiC of appropriate doping and thickness is placed underneath a GaN layer. GaN leads to improved switching performance of the device, while SiC accounts for the required breakdown voltage and heat dissipation. Static and switching performance of the 10 kV hybrid device 30 is shown in FIGs. 8, 10 and 12 and can be compared with static and switching performance of 4.5 kV devices 10 in FIGs. 7, 9 and 11.

The hybrid device 30 shows a kink in its forward I-V characteristics (FIG. 10) which has no influence on its

performance. This kink is attributed to the delay in the onset of high-level injection in the drift region due to noticeable differences in carrier lifetime and mobility across the heterojunction. Table III shows the energy losses associated with switching of the hybrid device 30. The hybrid device 30, thus, achieves a compromise between the low switching losses of GaN and high thermal conductivity of SiC.

FIG. 13 depicts a metal insulated semiconductor field effect transistor (MISFET) 50 constructed in accordance with another embodiment of the invention. Under the embodiment, the n+ type substrate 54 of GaN and n-type drift region 52 are fabricated using an epitaxial process described above for the diode 10 with doping levels of 2e16 and 1e16 $cm^{-3}$, respectively.

The p-type layer 56 may also be fabricated using an epitaxial process. The doping level of the p-type layer would be on the level of 1e17 $cm^{-3}$.

Following the creation of the p-type layer 56, the MISFET 50 is completed using mainly a combination of etching and diffusion steps. First, the p-type layer 56 is masked and etched to expose the region over the n+ type 58. A - material may be implanted over the exposed area. The material may then be heated to diffuse the n material into the base creating the n+ area 58 with a doping level of approximately 1e19 $cm^{-3}$.

Next, the surface may again be masked and exposed in the area over the trench. Once exposed, the trench may be etched to the proper depth. The surface may again be masked to expose the area surrounding the trench. The AlN insulating layer 60 may then be laid down over the exposed area using sputtering or an epitaxial process.

Once more, the area may be masked to create the gate 62 and external connections to the gate 62. The trench may then be refilled with polysilicon or amorphous silicon. The trench refill step may also be performed using an epitaxial deposition of alternate materials.

Following the trench refill, the device must again be masked and exposed to reveal a somewhat larger area around the gate 62. A dielectric 64 (e.g., AlN) may be laid down over the area again using an epitaxial process. The process may be completed by laying down a metal layer 66, 68 to create the source and drain connections.

In another embodiment, a n+ type SiC substrate 78 is used as shown in FIG. 14 to control injection efficiency and improve heat transfer. The substrate 78 and drift region may be created as described for the diode 30 of FIG. 2. The channel region 76 and n+ region 88, insulator 80 and gate 82 may be laid down as described for the MISFET of FIG. 13.

The n+ type SiC substrate 78 would be expected to have a doping level of 1e19 $cm^{-3}$. The n-type GaN drift region 72 would have a doping level of 1e16 $cm^{-3}$. The p-type GaN channel region 76 would have a doping level of 1e17 $cm^{-3}$. The n+ type GaN region 88 would have a doping level of 1e19 $cm^{-3}$.

In another embodiment of the invention, a n-type SiC buffer region 93 is provided in the MISFET 90 of FIG. 15 to further improve injection efficiency and improve the reverse recovery of the parasitic pn junction diode. The device 90 would be fabricated substantially the same as the device 70 of FIG. 14, but with the addition of an extra step of growing the buffer layer 93. The buffer layer 93 would be grown epitaxially or by CVD and would be expected to have a doping level of 2e17 $cm^{-3}$.

In another embodiment of the invention, an IGBT 120 (FIG. 16) is provided using GaN as a charge control material. The IGBT 120 may be fabricated as described for FIG. 13. One exception, however, is that the substrate 124 becomes a p+ layer 124 instead of the n+ layer 54 described in FIG. 13.

In another embodiment, an IGBT 140 is provided with a GaN drift region 142 on a SiC substrate 144. The device 140 may be fabricated using the process described in conjunction with FIG. 14, with the exception of substituting a p+ substrate 144 as a starting material.

In another embodiment, an IGBT 160 is provided with a GaN drift region 62, a buffer layer 164 fabricated on a SiC substrate 165. The device 160 may be fabricated using the process described in conjunction with FIG. 15, with the exception of substituting a p+ substrate 168 as a starting material.

In another embodiment of the invention, the MISFETs 50, 70, 90 of FIGs. 13, 14, 15 and IGBTs 120, 140 and 160 of FIGs. 16, 17, 18 have exposed channel regions 56, 76, 96, 126, 146 and 166 for optical triggering. While it is anticipated that any bright photon source would trigger the devices, it is anticipated that the devices would be especially susceptible to laser triggering. Such a device would be especially useful in high voltage applications (e.g., the power generating industry) where isolation of the gate lead is difficult or impossible.

Specific embodiments of novel apparatus for fabricating high voltage, low-loss semiconductors using Periodic Table Group III nitrides according to the present invention have been described for the purpose of illustrating the manner in which the invention is made and used. It should be understood that the implementation of other variations and

modifications of the invention and its various aspects will be apparent to one skilled in the art, and that the invention is not limited by the specific embodiments described. Therefore, it is contemplated to cover the present invention any and all modifications, variations, or equivalents that fall within the true spirit and scope of the basic underlying principles disclosed and claimed herein.

CLAIMS

1. A semiconductor charge-control device comprising:

a first layer of a Periodic Table Group III nitride of a first conductivity type and a first doping level which forms a drift region of the semiconductor charge-control device;

a second layer of the Periodic Table Group III nitride of a second conductivity type and a second doping level at least one order of magnitude above the first doping level said second layer being disposed on a first side of the first layer; and

a third layer of the Periodic Table Group III nitride of the first conductivity type and a doping level of at least twice the doping level of the first layer, said third layer being disposed on the second side of the first layer.

2. The semiconductor device as in claim 1 wherein the Periodic Table Group III nitride further comprises gallium nitride.

3. The semiconductor device as in claim 1 wherein the third layer further comprises a device cathode.

4. The semiconductor device as in claim 1 wherein the second layer comprises an anode.

5. The semiconductor device as in claim 1 further comprising a fourth layer of the Periodic Table Group III nitride of the first conductivity type and a doping level at least two orders of magnitude higher than the doping level of the second layer, said fourth layer being disposed over the second layer.

6. The semiconductor device as in claim 1 further comprising a trench gate at least partially disposed over the fourth layer and penetrating the third and fourth layers and at least partially penetrating the first layer.

7. The semiconductor device as in claim 1 further comprising an aluminum nitride layer insulating the trench gate from the first, third and fourth layers.

8. The semiconductor device as in claim 1 further comprising a conductive metallic layer disposed over a portion of the fourth layer.

9. A semiconductor device comprising:

a first layer of a Periodic Table Group III nitride of a first conductivity type and a first doping level which forms a drift region of the semiconductor device;

a second layer of the Periodic Table Group III nitride of a second conductivity type and a second doping level at least one order of magnitude above the first doping level said second layer being disposed on a first side of the first layer; and

a third layer of silicon carbide of the first conductivity type and a different doping level, said third layer being disposed on the second side of the first layer.

10. The semiconductor device as in claim 9 wherein the Periodic Table Group III nitride further comprises gallium nitride.

11. The semiconductor device as in claim 9 wherein the third layer further comprises a device cathode.

12. The semiconductor device as in claim 9 wherein the second layer comprises an anode.

13. The semiconductor device as in claim 9 further comprising a fourth layer of the Periodic Table Group III nitride of the first conductivity type and a doping level at least two orders of magnitude higher than the doping level of the second layer, said fourth layer being disposed over the second layer.

14. The semiconductor device as in claim 9 further comprising a trench gate at least partially disposed over the fourth layer and penetrating the third and fourth layers and at least partially penetrating the first layer.

15. The semiconductor device as in claim 9 further comprising an aluminum nitride layer insulating the trench gate from the first, third and fourth layers.

16. The semiconductor device as in claim 9 further comprising a conductive metallic layer disposed over a portion of the fourth layer.

17. An insulated gate bipolar transistor comprising:

a first layer of Galium nitride of a first conductivity type and a first doping level which forms a portion of the drift region of the bipolar transistor;

a second layer of the Galium nitride of a second conductivity type and a second doping level at least one order of magnitude above the first doping level said second layer being disposed on a first side of the first layer;

a third layer of silicon carbide of the first conductivity type and a doping level different from the

first layer, said third layer being disposed on the second side of the first layer;

a fourth layer of the Periodic Table Group III nitride of the first conductivity type and a doping level at least two orders of magnitude higher than the doping level of the second layer, said fourth layer being disposed over the second layer;

a trench gate at least partially disposed over the fourth layer and penetrating the third and fourth layers and at least partially penetrating the first layer;

an aluminum nitride layer insulating the trench gate from the first, third and fourth layers; and

a conductive metallic layer disposed over a portion of the fourth layer.

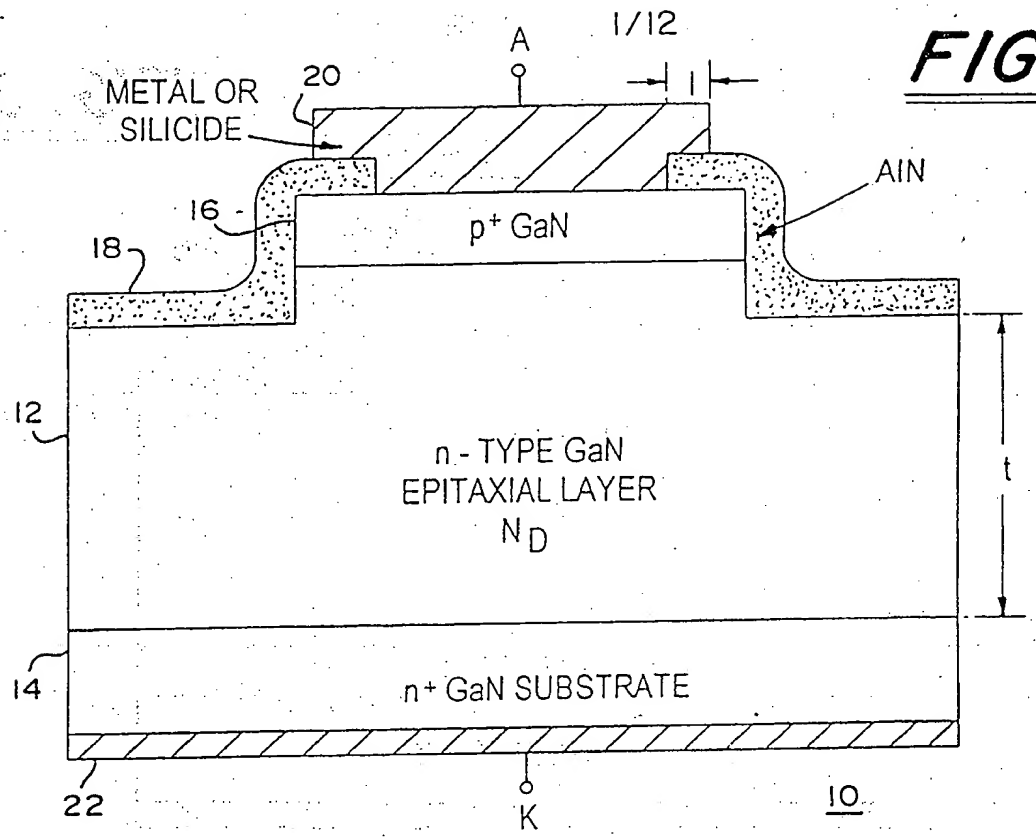



FIG. 1

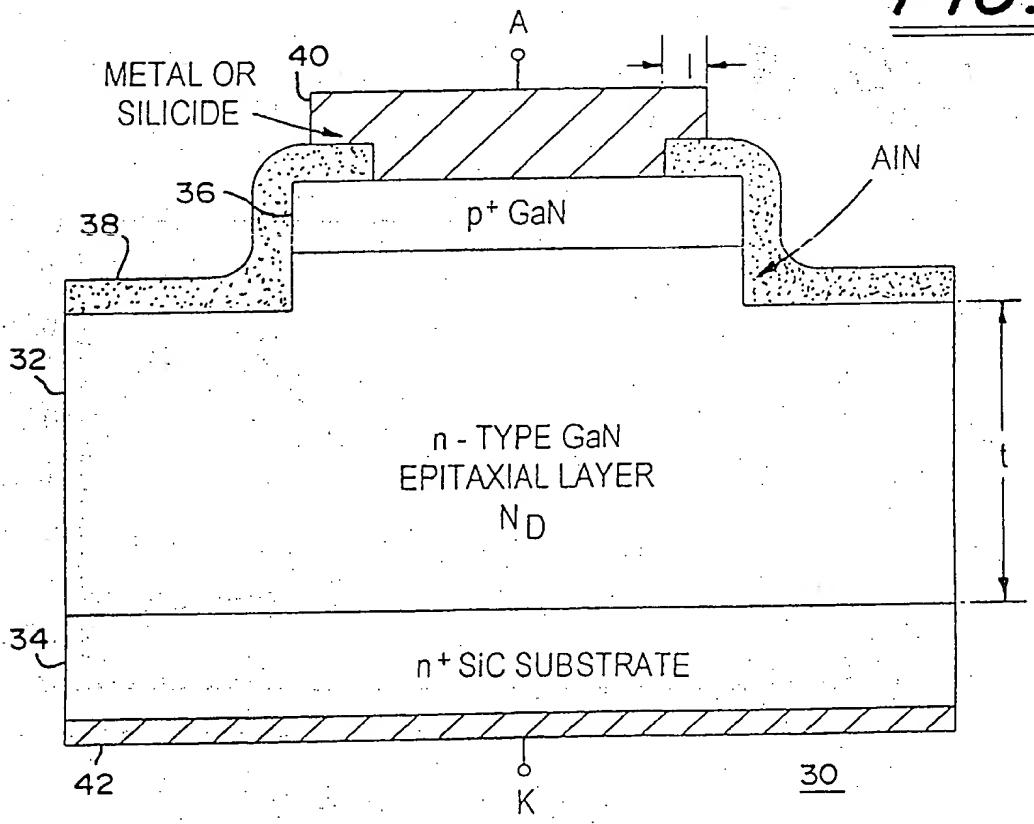



FIG. 2

FIG. 3

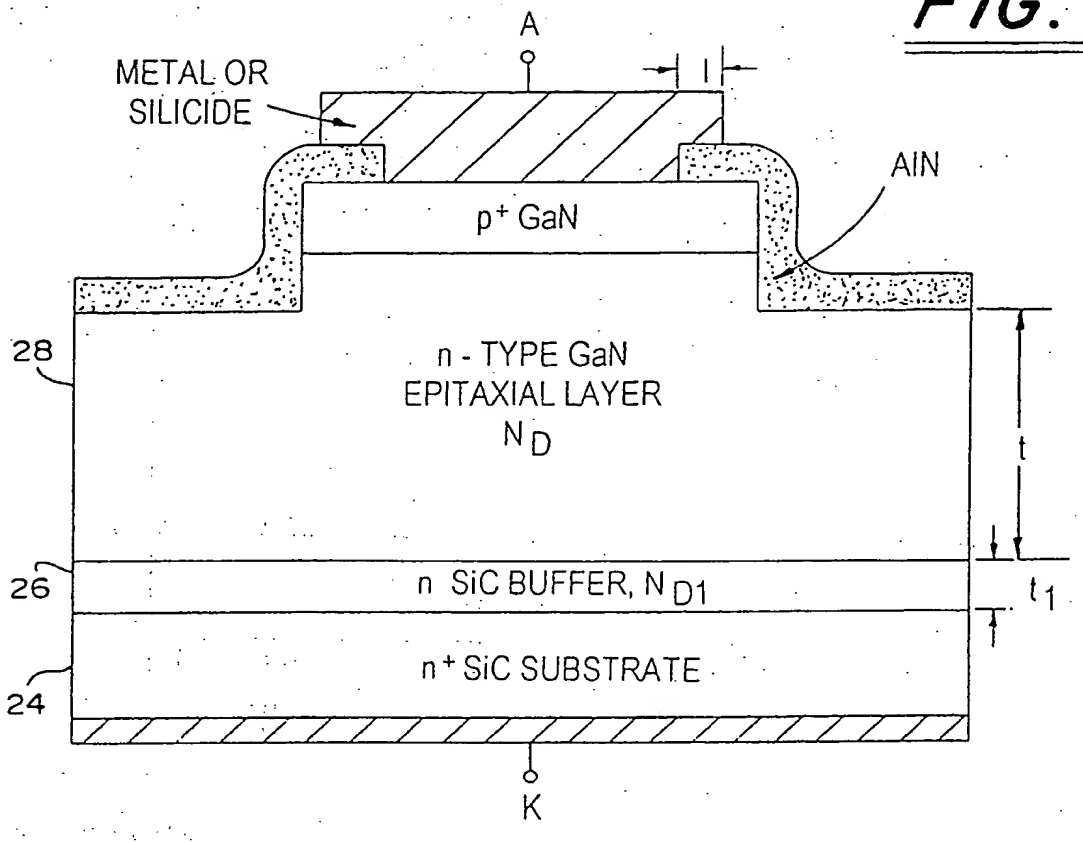

A
l
METAL OR
SILICIDE
AlN
p+ GaN
28
n - TYPE GaN
EPITAXIAL LAYER
N D
t
26
n SiC BUFFER, N D1
t 1
n+ SiC SUBSTRATE
24
K

FIG. 4

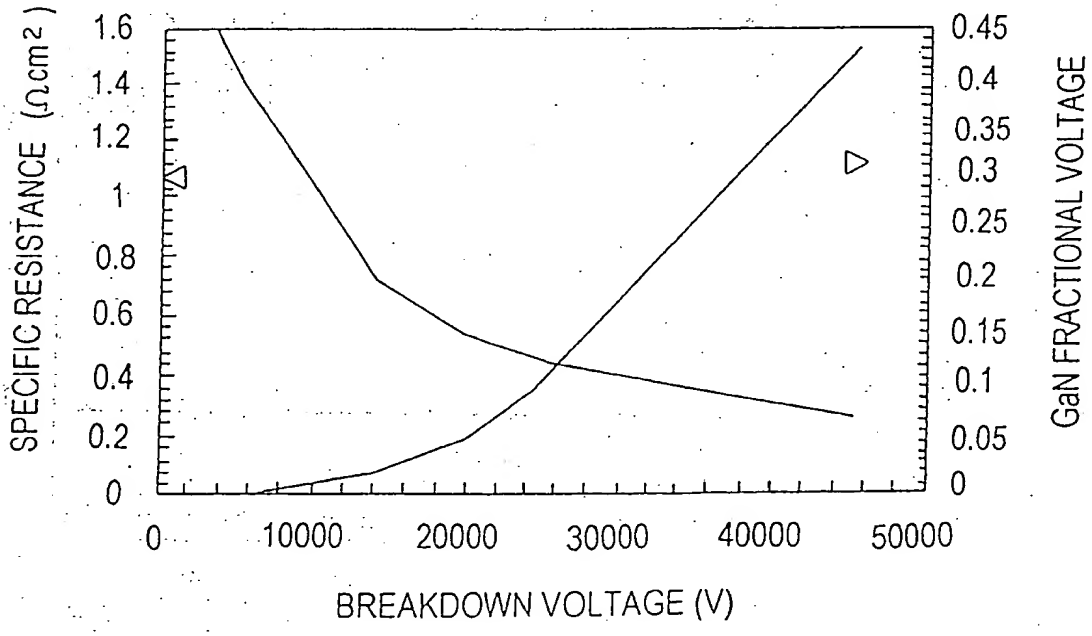

SPECIFIC RESISTANCE (Ω.cm2)
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
GaN FRACTIONAL VOLTAGE
0
10000
20000
30000
40000
50000
BREAKDOWN VOLTAGE (V)

FIG. 5

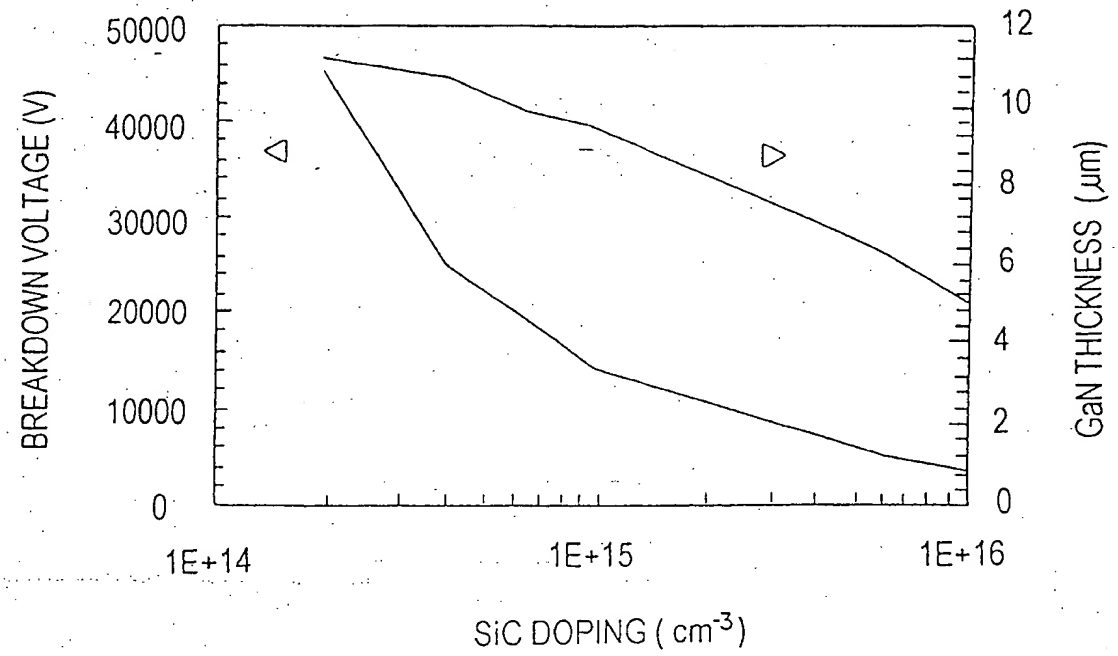

50000
40000
30000
20000
10000
0
BREAKDOWN VOLTAGE (V)
12
10
8
6
4
2
0
GaN THICKNESS (μm)
1E+14
1E+15
1E+16
SiC DOPING ( cm-3)

FIG. 6

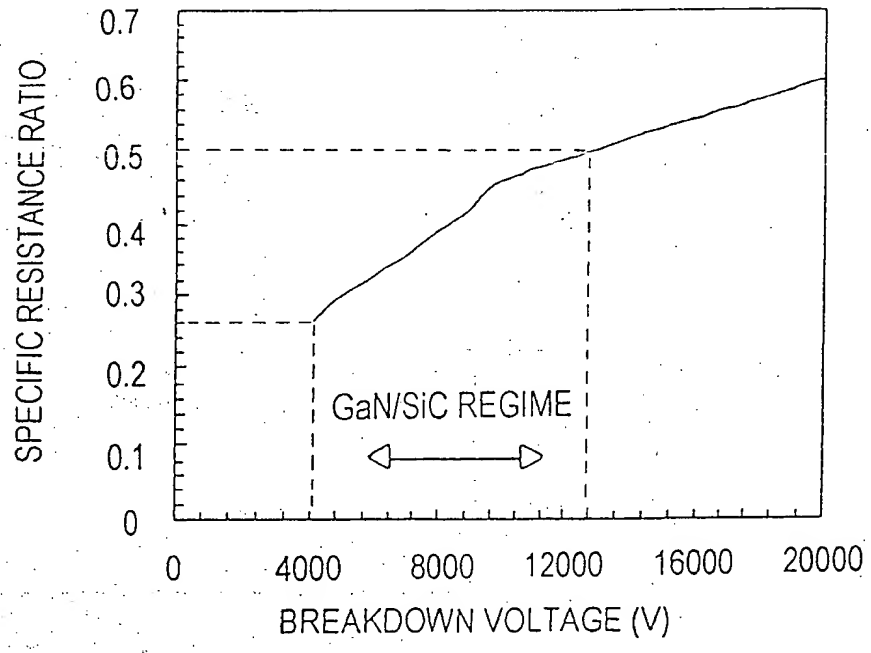

0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
SPECIFIC RESISTANCE RATIO
GaN/SiC REGIME
0
4000
8000
12000
16000
20000
BREAKDOWN VOLTAGE (V)

FIG. 7

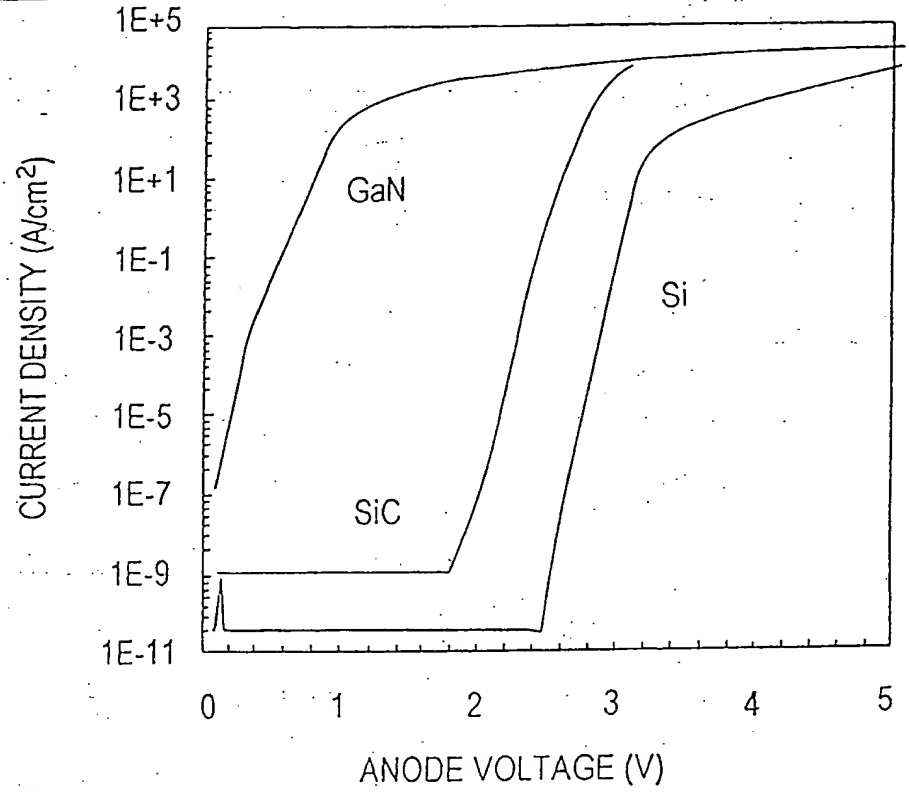

1E+5
1E+3
1E+1
1E-1
1E-3
1E-5
1E-7
1E-9
1E-11
CURRENT DENSITY (A/cm²)
GaN
Si
SiC
0
1
2
3
4
5
ANODE VOLTAGE (V)

FIG. 8

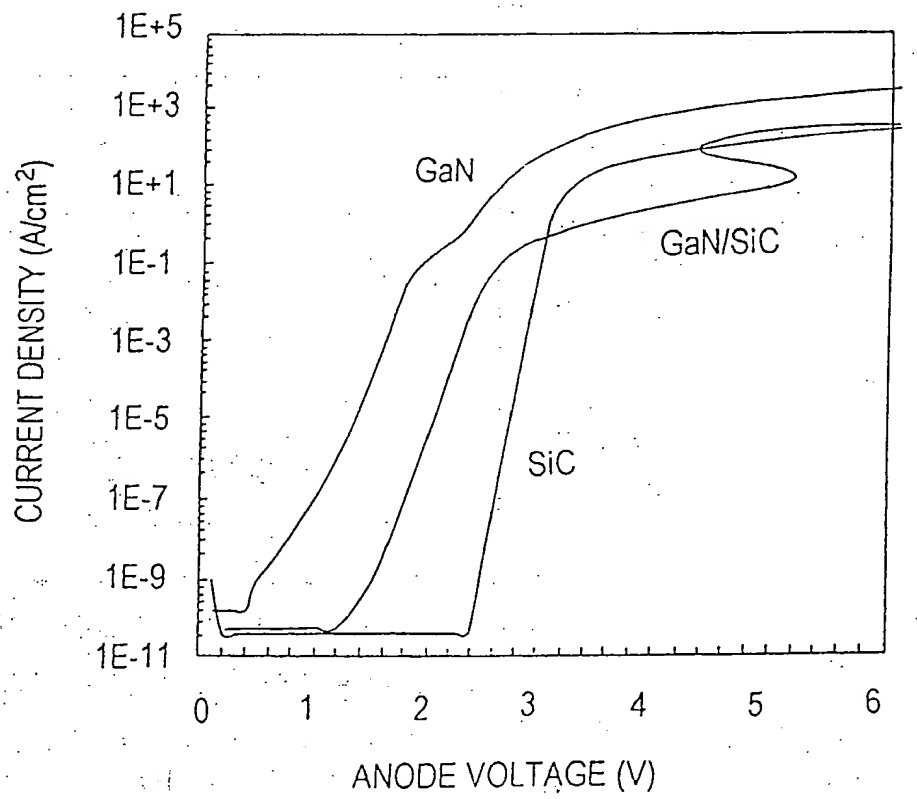

1E+5
1E+3
1E+1
1E-1
1E-3
1E-5
1E-7
1E-9
1E-11
CURRENT DENSITY (A/cm²)
GaN
GaN/SiC
SiC
0
1
2
3
4
5
6
ANODE VOLTAGE (V)

FIG. 9

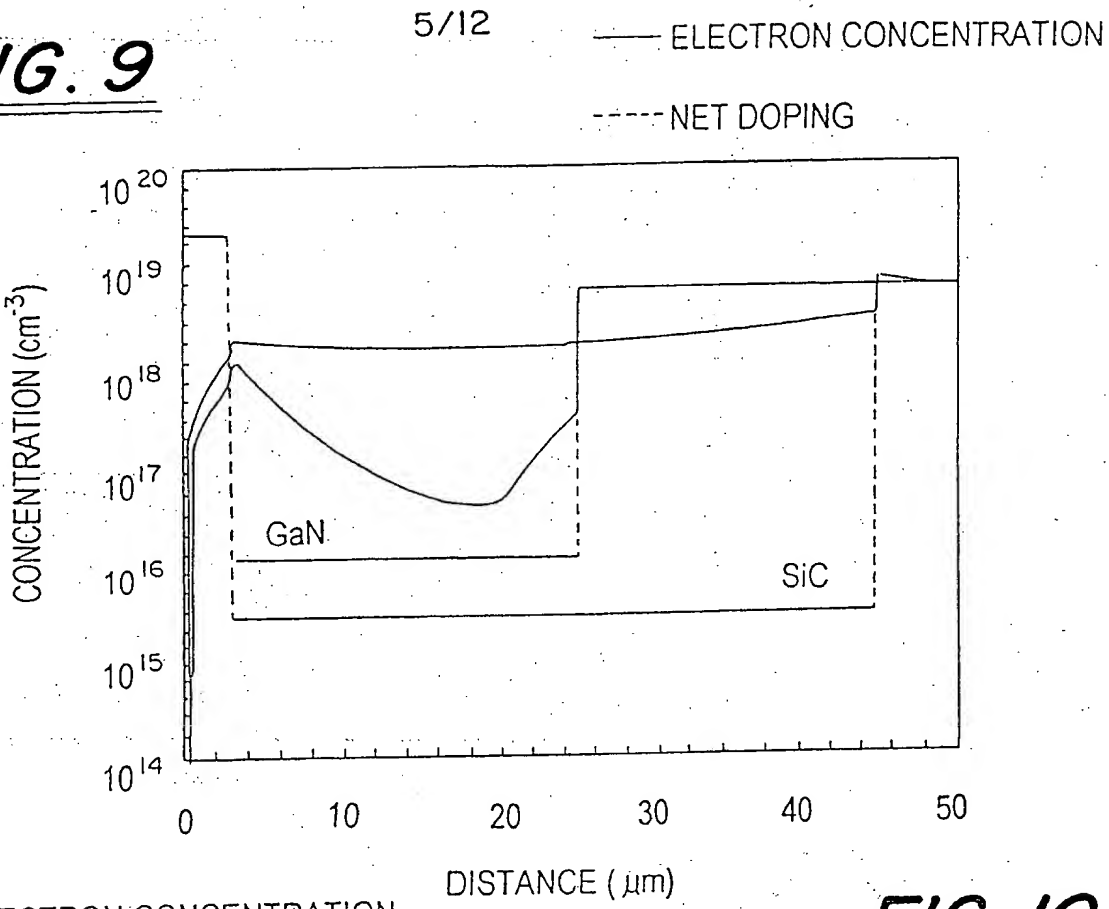

ELECTRON CONCENTRATION
NET DOPING
CONCENTRATION (cm-3)
10 20
10 19
10 18
10 17
10 16
10 15
10 14
GaN
SiC
0
10
20
30
40
50
DISTANCE (μm)

FIG. 10

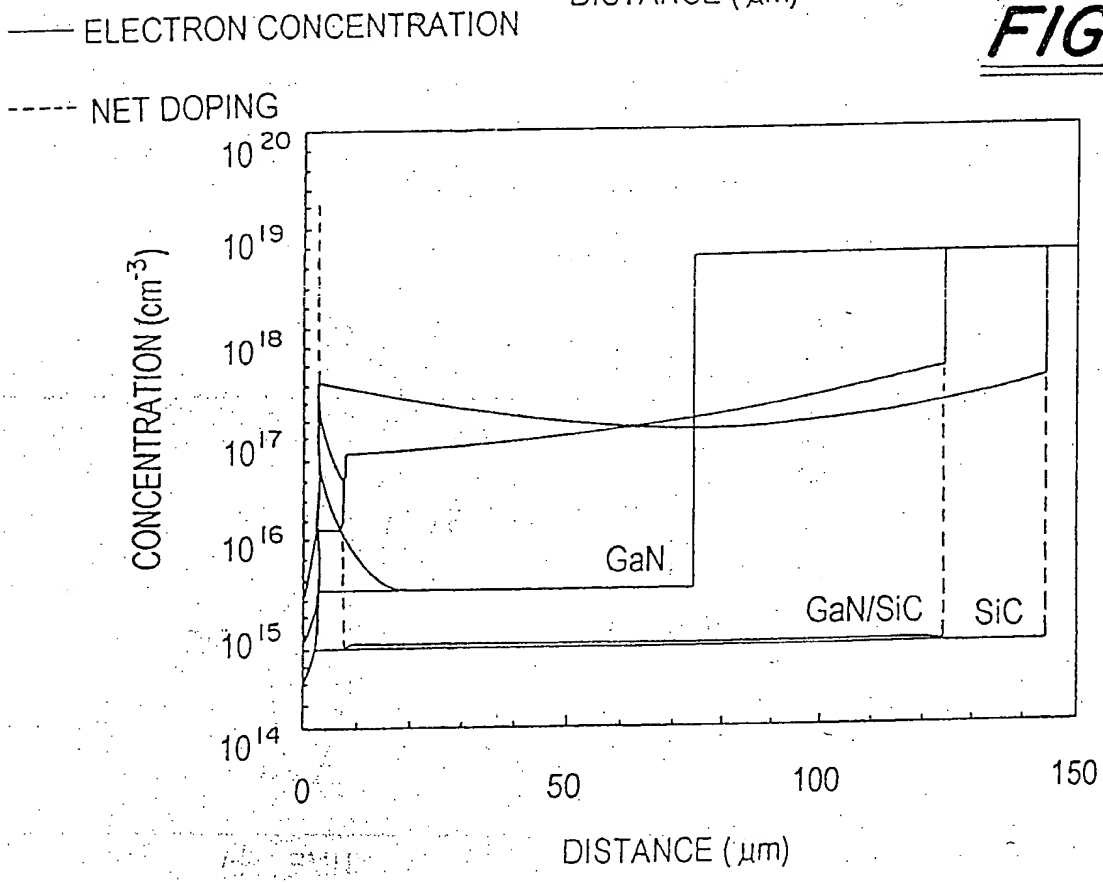

ELECTRON CONCENTRATION
NET DOPING
CONCENTRATION (cm-3)
10 20
10 19
10 18
10 17
10 16
10 15
10 14
GaN
GaN/SiC
SiC
0
50
100
150
DISTANCE (μm)

FIG. 11

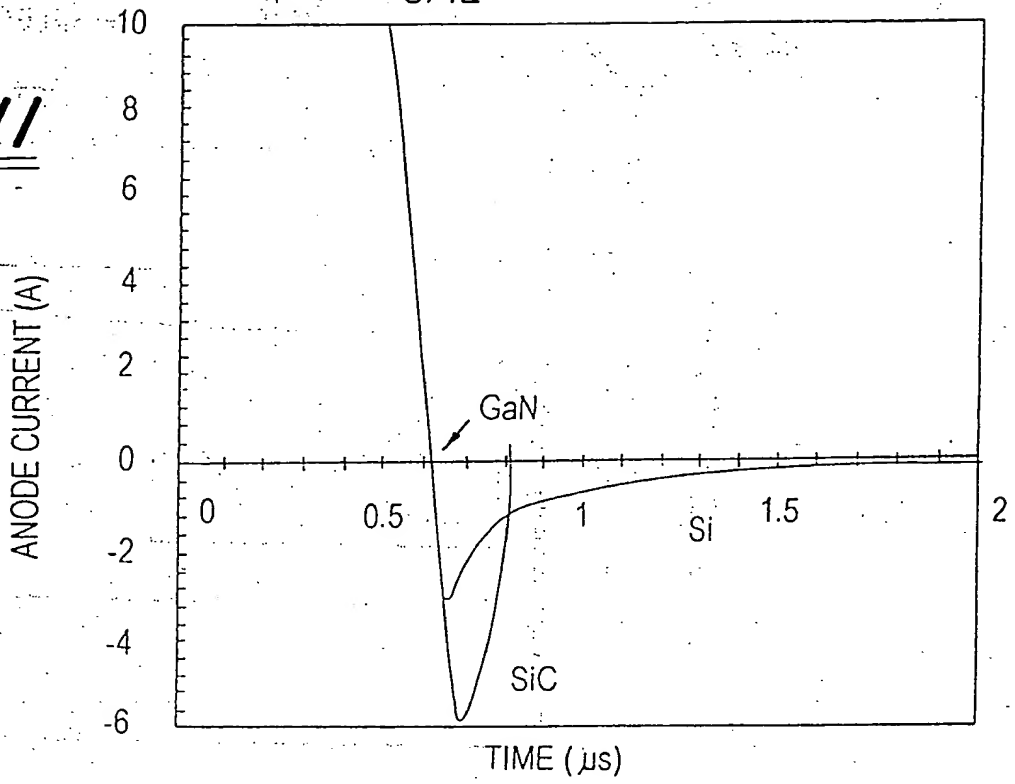

ANODE CURRENT (A)
10
8
6
4
2
0
-2
-4
-6
0
0.5
1
1.5
2
GaN
Si
SiC
TIME (μs)

FIG. 12

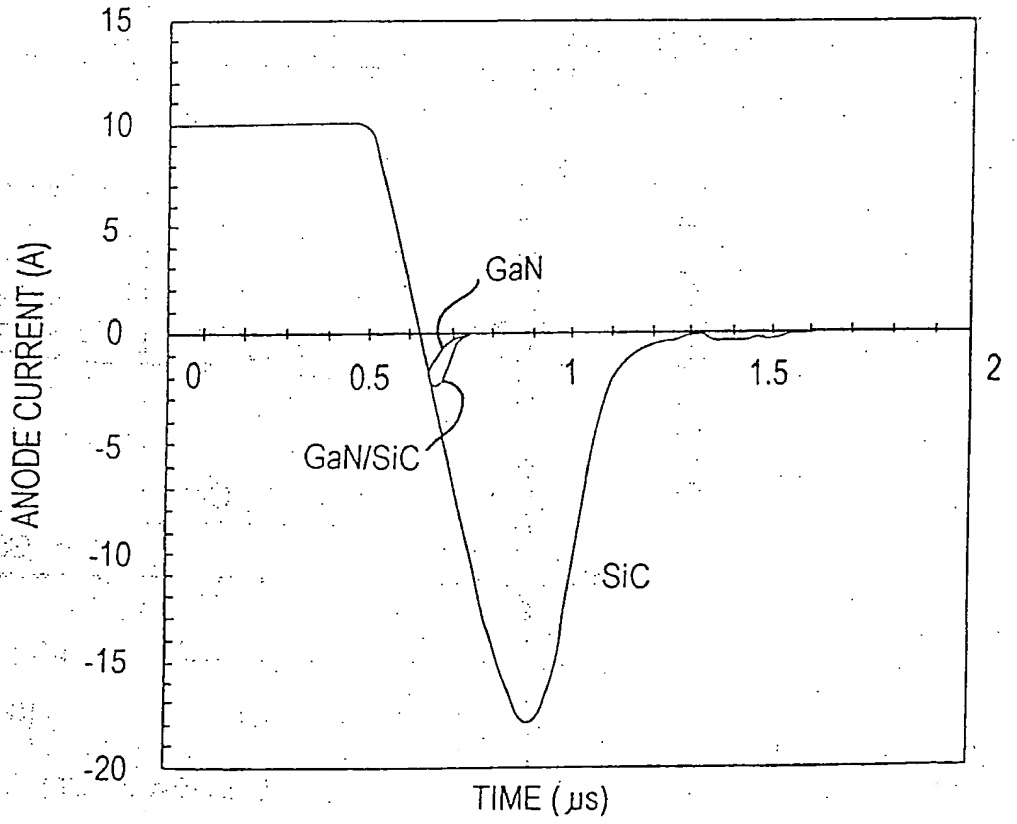

ANODE CURRENT (A)
15
10
5
0
-5
-10
-15
-20
0
0.5
1
1.5
2
GaN
GaN/SiC
SiC
TIME (μs)

FIG. 13

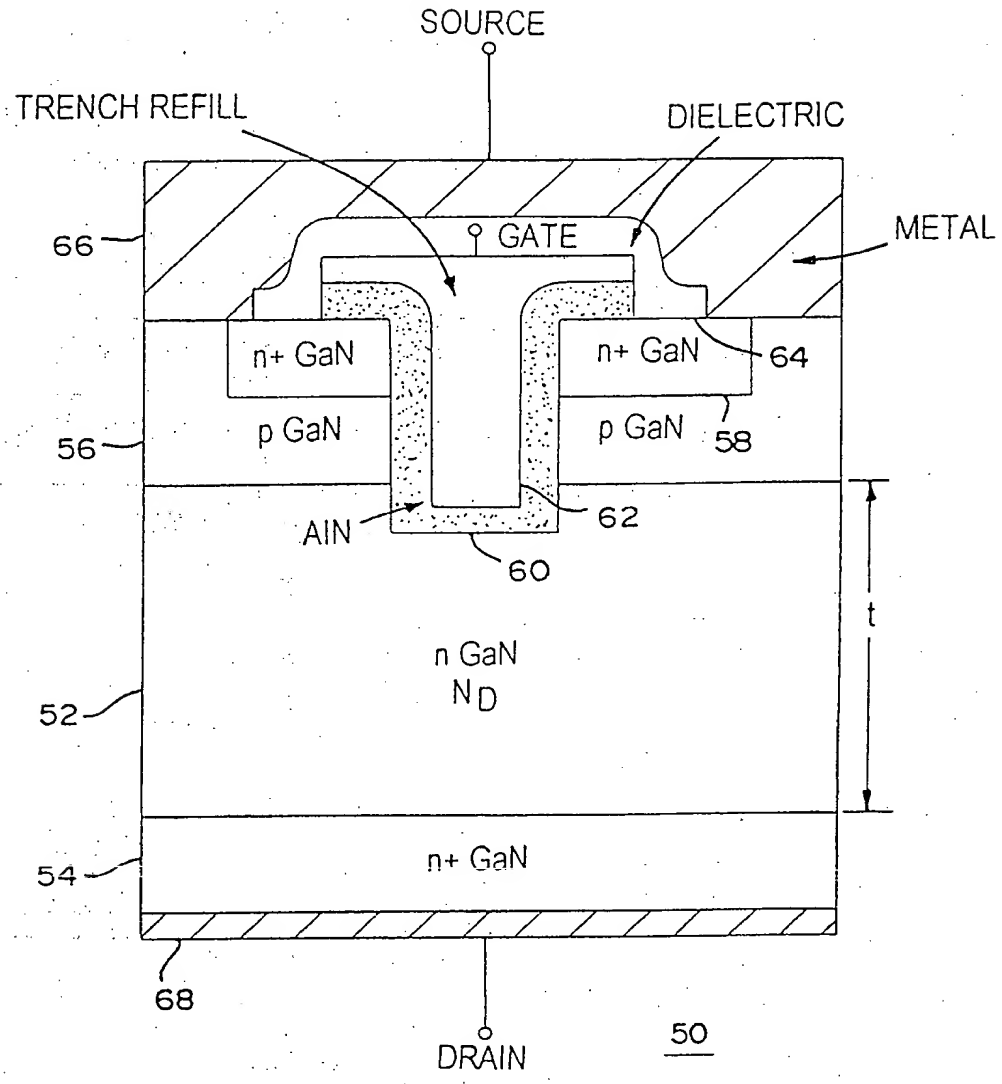

SOURCE
TRENCH REFILL
DIELECTRIC
METAL
GATE
66
n+ GaN
n+ GaN
64
p GaN
p GaN
58
56
AlN
62
60
t
n GaN
$N_D$
52
n+ GaN
54
68
DRAIN
50

FIG. 14

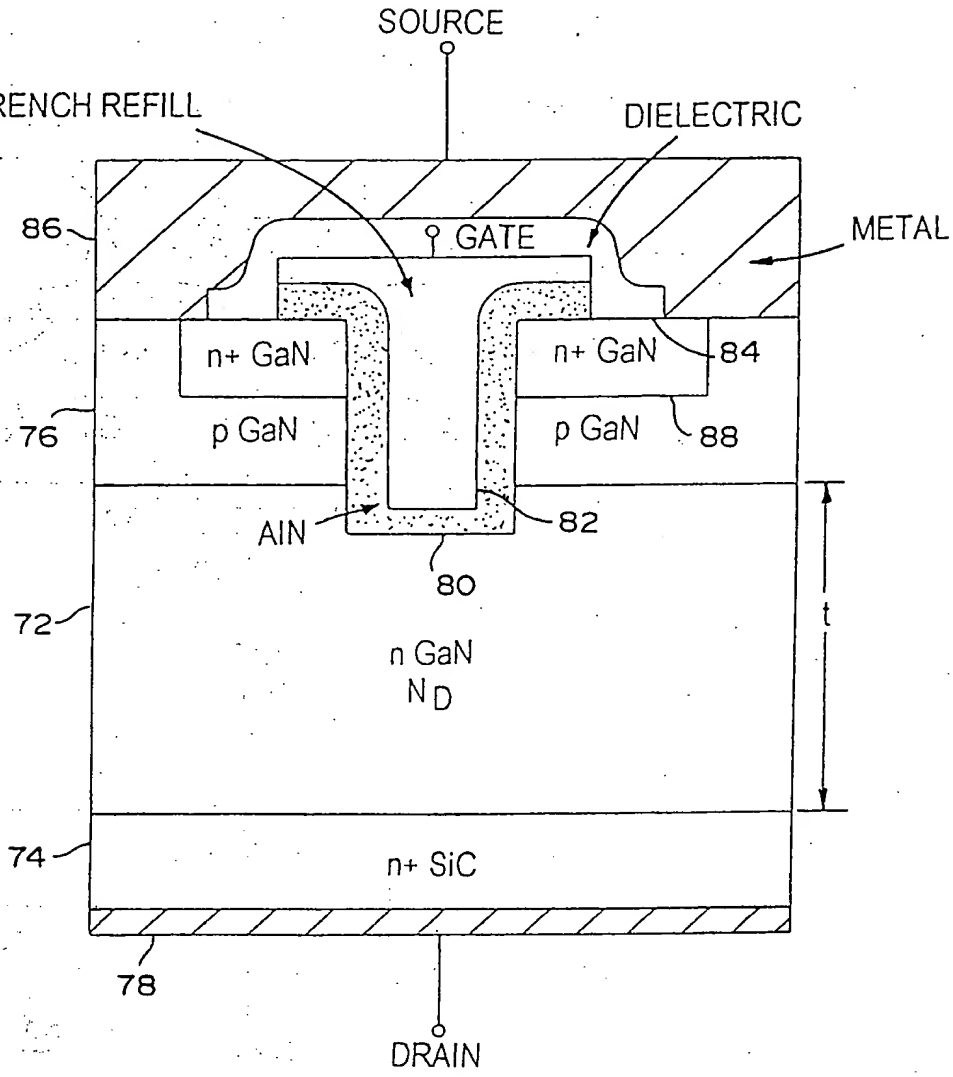

SOURCE
TRENCH REFILL
DIELECTRIC
86
GATE
METAL
n+ GaN
n+ GaN
84
76
p GaN
p GaN
88
AlN
82
80
72
n GaN
$N_D$
t
74
n+ SiC
78
DRAIN
70

FIG. 15

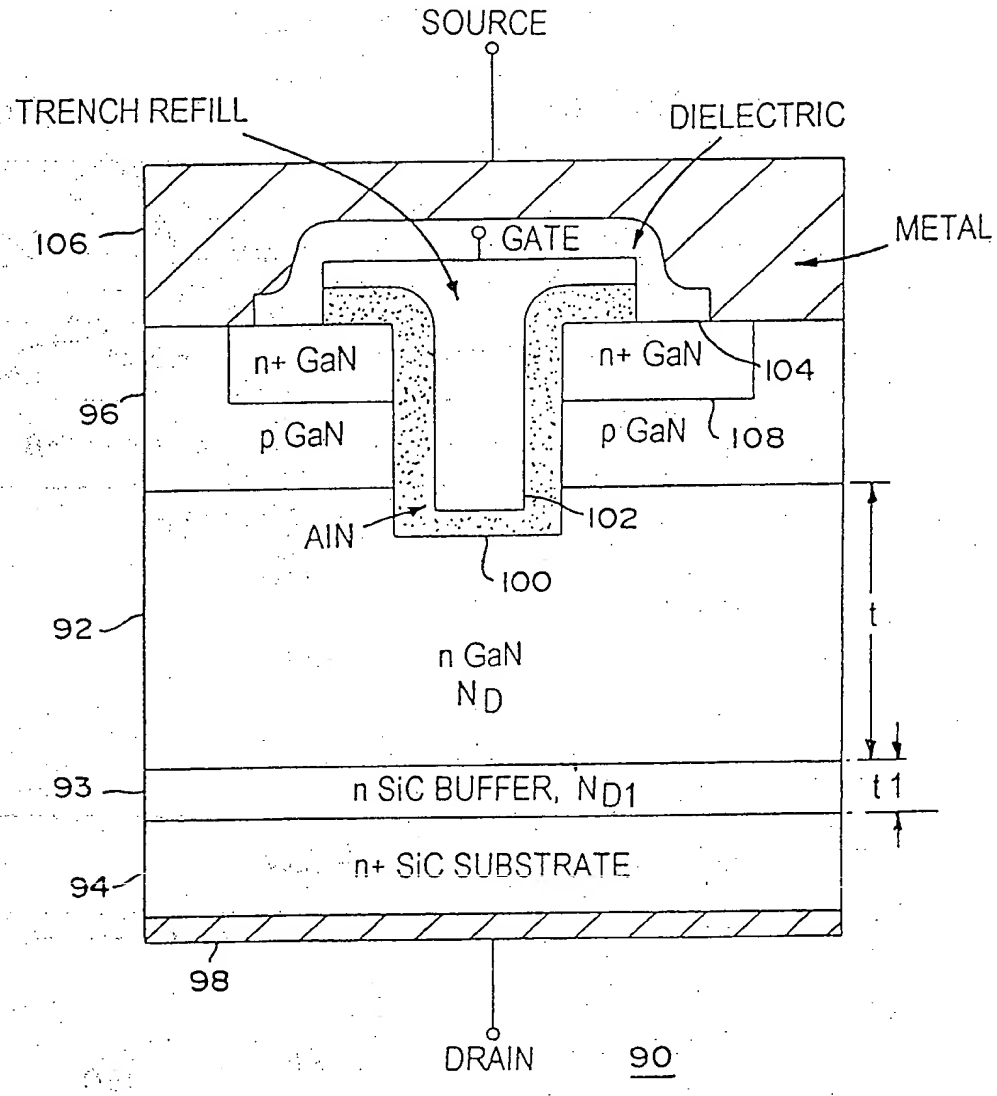

SOURCE
TRENCH REFILL
DIELECTRIC
METAL
GATE
106
n+ GaN
n+ GaN
104
96
p GaN
p GaN
108
AlN
102
100
92
n GaN
$N_D$
t
93
n SiC BUFFER, $N_{D1}$
t1
94
n+ SiC SUBSTRATE
98
DRAIN
90

FIG. 16

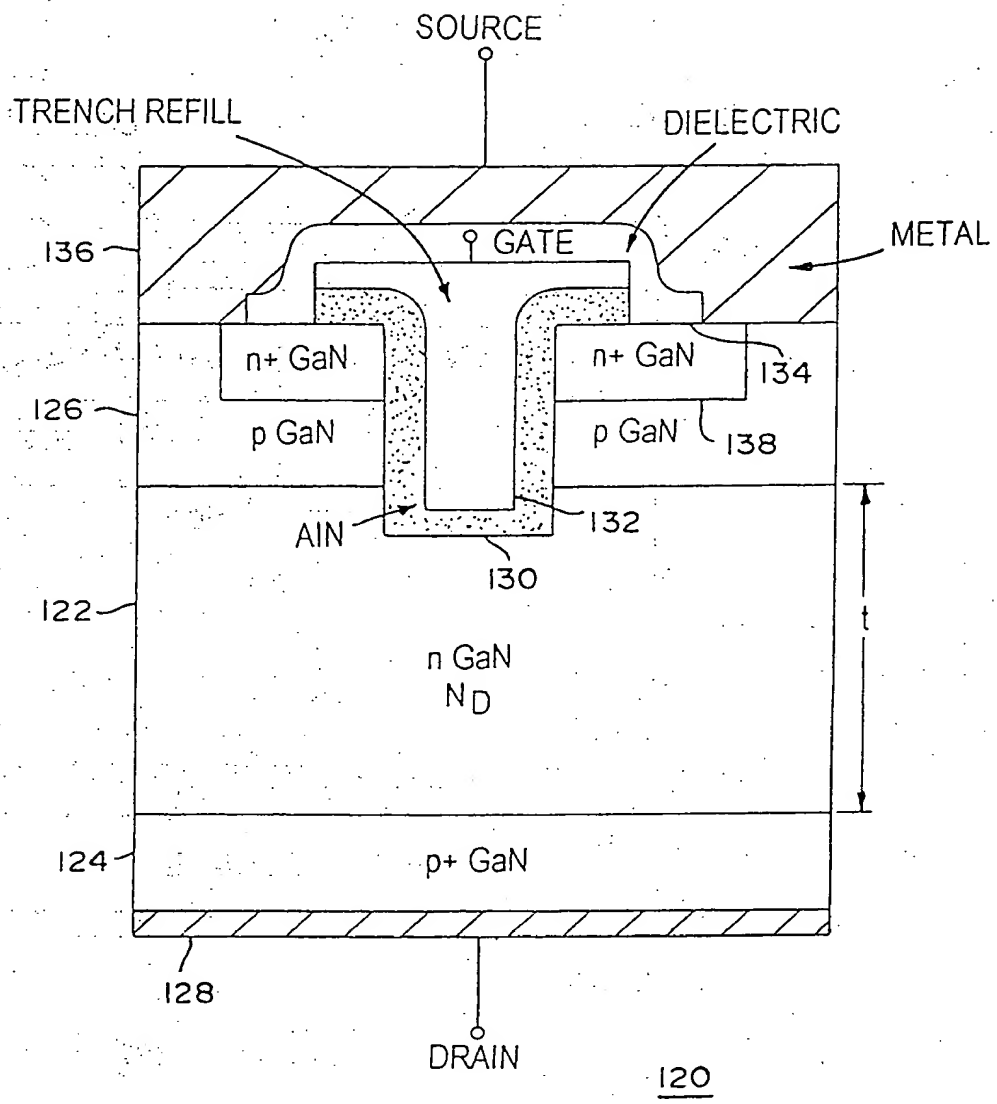

SOURCE
TRENCH REFILL
DIELECTRIC
METAL
GATE
136
n+ GaN
n+ GaN
134
126
p GaN
p GaN
138
AlN
132
130
122
n GaN
$N_D$
t
124
p+ GaN
128
DRAIN
120

FIG. 17

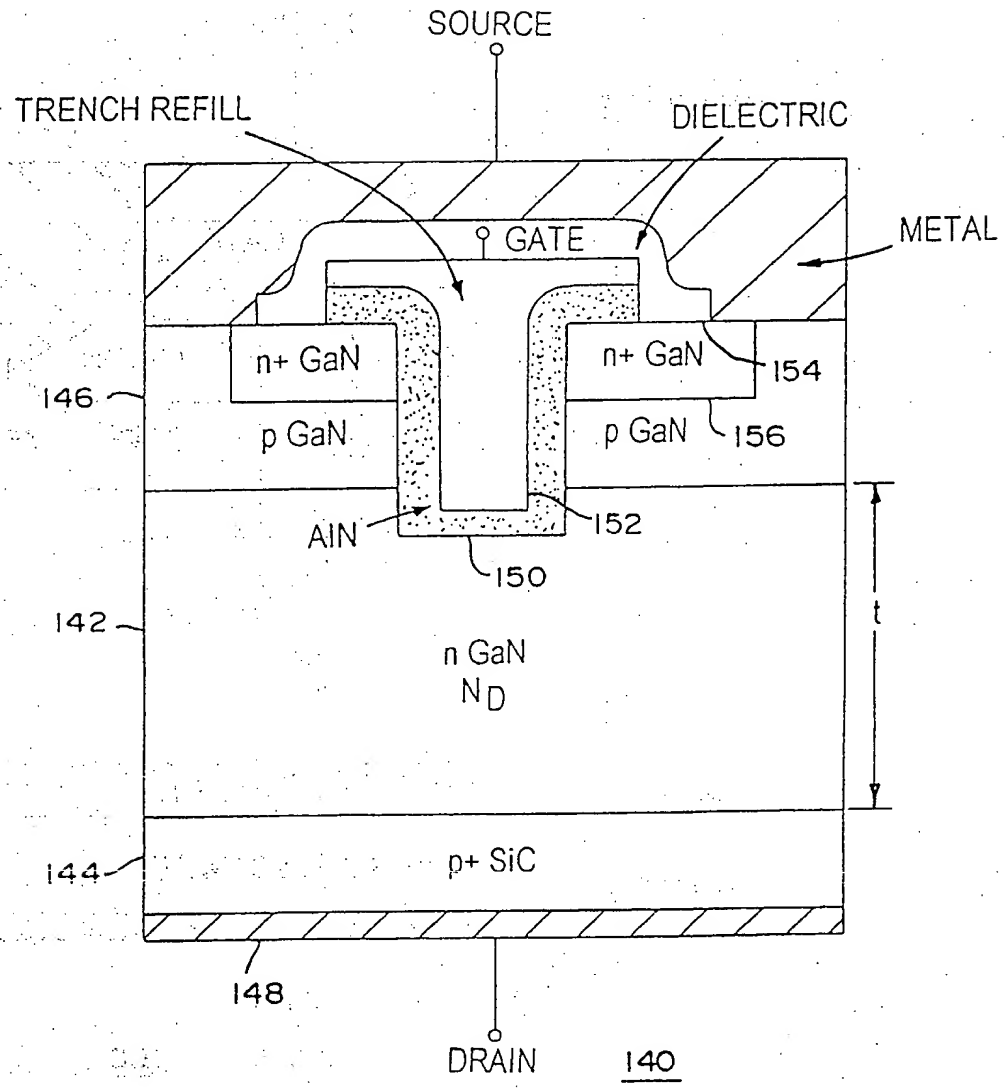
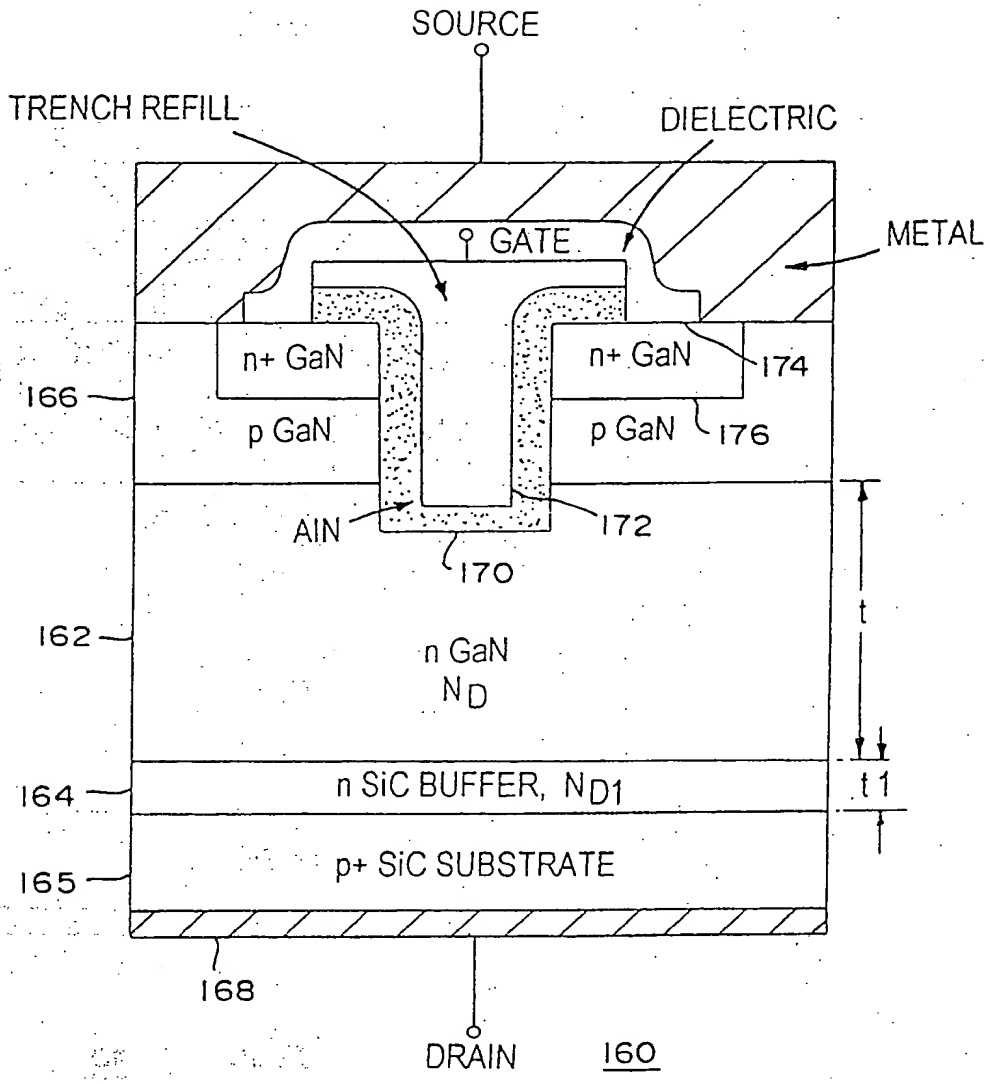

SOURCE
TRENCH REFILL
DIELECTRIC
METAL
GATE
n+ GaN
n+ GaN
154
146
p GaN
p GaN
156
AlN
152
150
142
n GaN
$N_D$
t
144
p+ SiC
148
DRAIN
140

FIG. 18


SOURCE
TRENCH REFILL
DIELECTRIC
METAL
GATE
n+ GaN
n+ GaN
174
166
p GaN
p GaN
176
AlN
172
170
t
162
n GaN
$N_D$
n SiC BUFFER, $N_{D1}$
t1
164
p+ SiC SUBSTRATE
165
168
DRAIN
160

# INTERNATIONAL SEARCH REPORT

Internatic application No.
PCT/US98/02856

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 31/0256
US CL :257/76, 107, 77
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/76, 107, 77, 109, 155, 168

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5,641,975 A (AGARWAL ET AL) 24 June 1997 (24/06/97), see figure 1B. | 1, 2, 9, 10 |
| A | US 5,657,335 A (RUBIN ET AL) 12 August 1997 (12/08/97), see entire document. | 1-17 |
| A | US 4,985,742 A (PANKOVE) 15 January 1991 (15/01/91), see entire document. | 1-17 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 11 MAY 1998 | 18 JUN 1998 |

| Name and mailing address of the ISA/US | Authorized officer |
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| Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231 | NATHAN KELLEY |
| Facsimile No. (703) 305-3230 | Telephone No. (703) 308-0956 |

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